REMARKS

The following remarks are in response to the Office Action of June 6, 2005, for which a one-month extension is hereby requested. The Office Action rejected claim 42 under 35 U.S.C. 102(b) as being anticipated by Park et al. (US patent number 5,768,188) and as being anticipated by Banks (US patent number 5,218,569). For the reasons given below, it is respectfully submitted that these rejections are both in error and improper. The Office Action objected to, but indicated the allowability of, claim 43.

35 U.S.C. 102(b) rejection based on Park

Concerning the substance of the rejection of claim 42 under 35 U.S.C. 102(b) as being anticipated by Park, this is believed to be in error for a number of reasons. Perhaps the main error is the Office Action's identification of the waveform in Park's figure 6 with the "staircase program-verify pulse". This is incorrect: Park's figure 6 shows a *programming* waveform, not a program-verify waveform; that is, it shows the pulses applied to the memory cells to change their state, not a sense waveform applied to the cells afterwards to determine whether the cells have reached their target state. (Also, it should be noted that the waveform of Park's figure 6 is not a staircase, but a set of discreet pulses.)

More specifically, the Office Action refers to the Park's figure 6 and its description at column 11, lines 56-67. Beginning at line 62, this states:

> The cycle (a) is repeated by a number of repetitions (for example, 5 times) determined when designing the memory device. Each program operation uses a *program voltage* incremented from that used in the prior programming operation ...

As the added emphasis indicates, what is shown in figure 6 is the *programming* pulses' waveform, not the verify waveform. The program-verify operation is performed *between* these pulses, as shown in more detail in figure 5, illustrating each of the (A), (B), and (C) cycles. For each of these cycles (corresponding to different data states), the verify operation is performed using a *single* level to verify only a *single* one of the states. Thus, it is respectfully submitted that Park has no disclosure of "a staircase program-verify circuit for providing a staircase program-verify pulse electrically coupled to the memory array and capable of concurrently program-verifying the plurality of multi-level-cell memory cells".

For at least any of these reasons, it is believed that a rejection of claim 42 under 35 U.S.C. 102(b) as being anticipated by Park is not well founded and should be withdrawn.

35 U.S.C. 102(b) rejection based on Banks

Concerning the substance of the rejection of claim 42 under 35 U.S.C. 102(b) as being anticipated by Banks, this is also believed to be in error for a number of reasons. Perhaps the main error is again the Office Action's identification of the bottom part of Banks' figure 11 with the "staircase program-verify pulse". This is incorrect: the bottom part of Banks' figure 11, which is more a series of ramps than a staircase, shows the *state of the memory cell in terms of its threshold value programming* in response to the programming waveform at the top of the figure, not a program-verify waveform provided to the memory; that is, it shows state of a memory cell in response to the pulses applied to the memory cell to change its state, not a sense waveform applied to the cell afterward each pulse to determine whether the cell has reached its target state.

More specifically, the Office Action refers to the Banks' figure 11 and its description at in column 11. As described beginning at line 14 of column 11, during the programming process (when the bit line and word line is taken high), charge is added to the floating gate. These are parts of lower figure that ramp up. In between these pulses, corresponding to the flat portion, is where the program-verify occurs *using a fixed reference voltage*, as described beginning at line 18 of column 11. In this particular figure, the cell is being programmed to the (1,0) state and is verified with the single, fixed program-verify voltage corresponding to this state, Vref3. At time t2 is when the level on the cell (shown by the series of ramps) verifies against this fixed program-verify reference value---which is again specific to a single target data state.

(The fact that the lower portion of figure 11 corresponds to the amount of charge on the memory cell (and, consequently, its threshold voltage) is reinforced by comparing figure 11 with figure 13. In figure 13, three programming pulses of decreasing length are used. This is then reflected in the bottom portion of figure 13, which shows three corresponding ramp portions of decreasing length.)

For at least any of these reasons, it is believed that a rejection of claim 42 under 35 U.S.C. 102(b) as being anticipated by Banks is not well founded and should be withdrawn.

On rejections under 35 U.S.C. 102 being improper

It is also respectfully submitted the Office Action's rejections of claim 42 under 35 U.S.C. 102(b) are improper and should be also withdrawn on this basis alone.

More specifically, the rejections made under 35 U.S.C. 102(b) against claim 42 can also be made on exactly the same basis against claim 1 of U.S. patent number 6,538,923: Claim 42 of

the present application is an exact copy of claim 1 of U.S. patent number 6,538,923 and the priority date of the present application is earlier than that of U.S. patent number 6,538,923. Consequently, the same rejections that the Office Action made under 35 U.S.C. 102(b) against claim 42 are equally applicable to claim 1 of U.S. patent number 6,538,923.

Claim 42 corresponds to claim 1 of U.S. patent number 6,538,923. More specifically, 42 is an exact copy of claim 1 of U.S. patent number 6,538,923 and has been placed into the present application for purposes of provoking an interference. (Similarly, claim 43 is an exact copy of claim 2 of U.S. patent number 6,538,923.) Consequently, the pending claims correspond to the claims of this patent and the provisions of section 2307.02 of the M.P.E.P. apply. As described in section 2307.02 of the M.P.E.P., the rejection of pending claim 42 based on grounds that are equally applicable to the claims of U.S. patent number 6,538,923 that correspond to the pending claims is improper and should be withdrawn.

In particular, the Examiner is referred to the second paragraph of section 2307.02 of the M.P.E.P.: As stated there, the prior art and 35 U.S.C. 112, second paragraph, rejections made in Office Action are improper and should be withdrawn. Such a rejection can be made only under particular circumstances. Specifically, as stated in the second paragraph of section 2307.02 of the M.P.E.P., "If the ground of rejection is also applicable to the corresponding claims in the patent, any letter including the rejection must have the approval of the TC Director." The Office Actions in the present application have not provided this special approval, are consequently improper, and should be withdrawn.

It is again noted that these Remarks of this section are not addressed to the substance of these rejections; rather, the argument is that this rejection is not proper under the particular processes of interference proceedings. Whether the rejections are, in fact, valid is another question, which, although discussed above, is more properly dealt with as part of the interference process. As noted in the last paragraphs of 37 CFR 41.201, a rejection under 35 U.S.C. 102 (b) is not listed among the threshold issues for determining whether to declare an interference. Thus, the rejections under 35 U.S.C. 102 (b) are not proper and should be o this basis alone withdrawn.

Conclusion

Consequently, for the reasons given above, it is respectfully submitted that the rejections under 35 U.S.C. 102 (b) are not well founded, and not proper, and should be withdrawn.

Respectfully submitted,

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